

FIG. 1

FIG. 2(a)

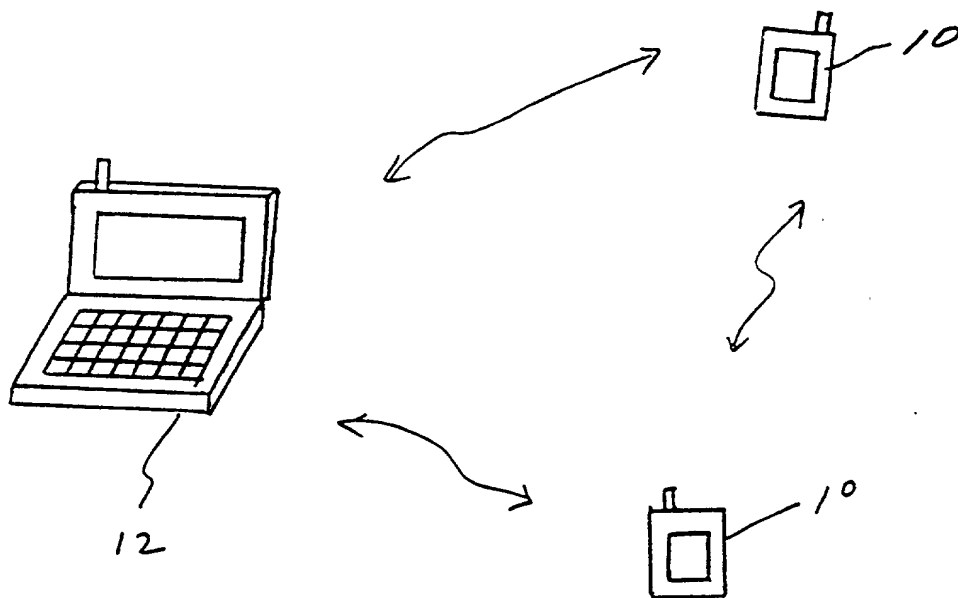
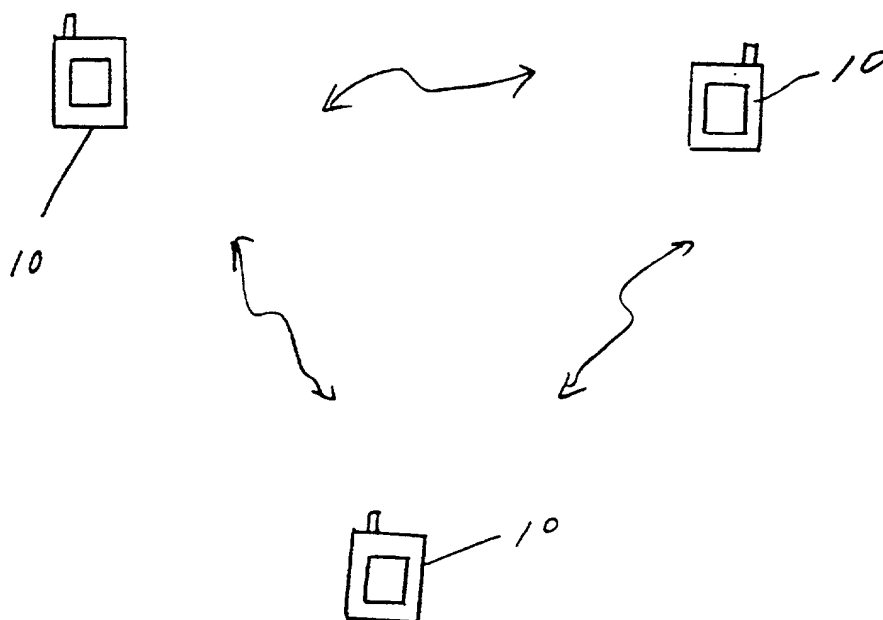


FIG. 2(b)



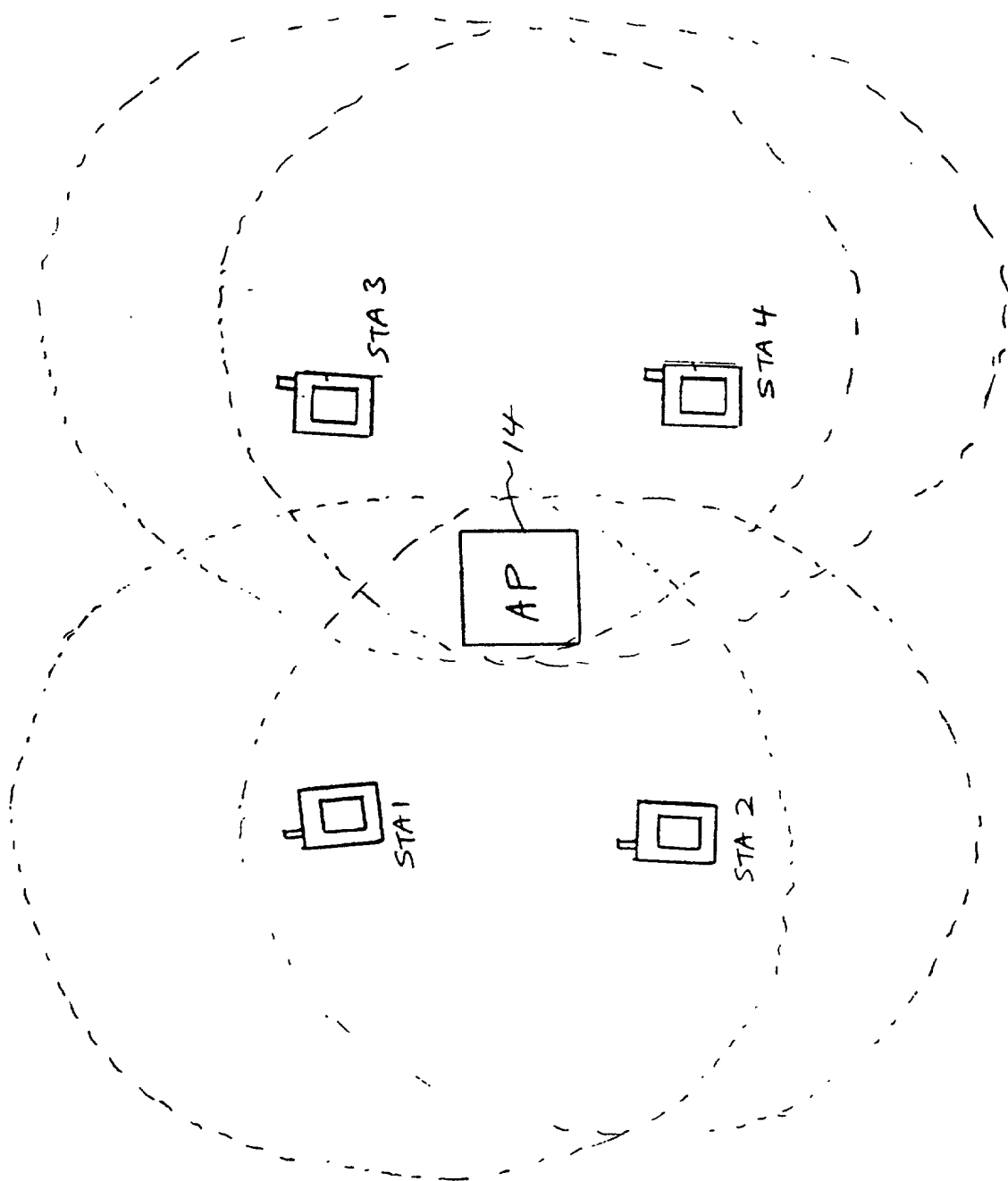


FIG. 3

FIG. 4 is a block diagram of a network interface device 14, which is connected to a network 16. The network interface device 14 includes a control unit 20, a memory unit 30, a transmit path 22, and a receive path 24. The transmit path 22 includes a multiplexer (Mux) Transmit 22, a transmit first-in first-out (TX FIFO) buffer 24, and a transmit/receive (TR/RX) interface 32. The receive path 24 includes a receive multiplexer (Mux) Receive 26, a receive first-in first-out (RX FIFO) buffer 28, and the TR/RX interface 32. The control unit 20 is connected to the memory unit 30, the TX FIFO buffer 24, the RX FIFO buffer 28, and the network 16. The network 16 is connected to a wireless LAN 36.

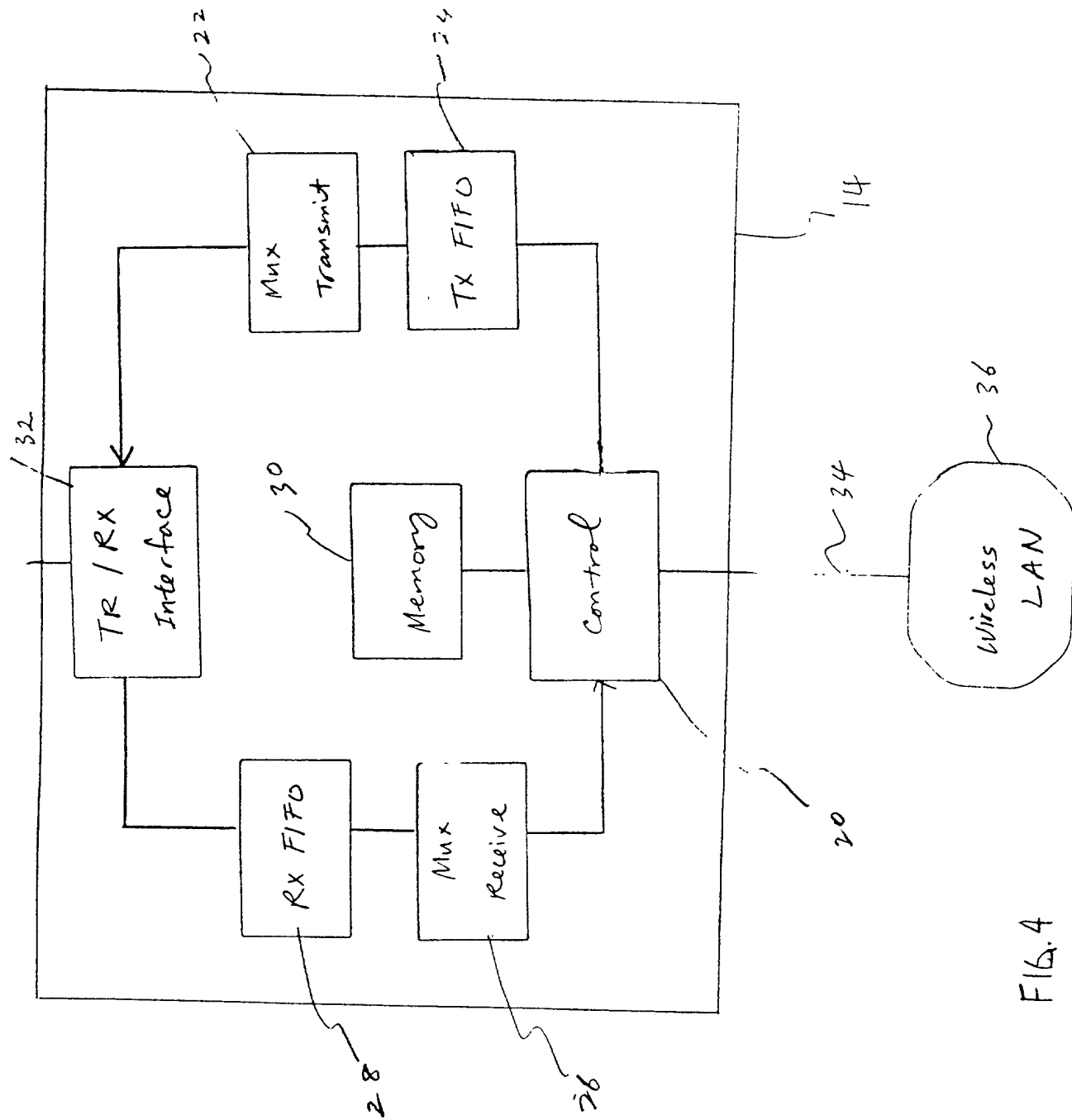


FIG. 4

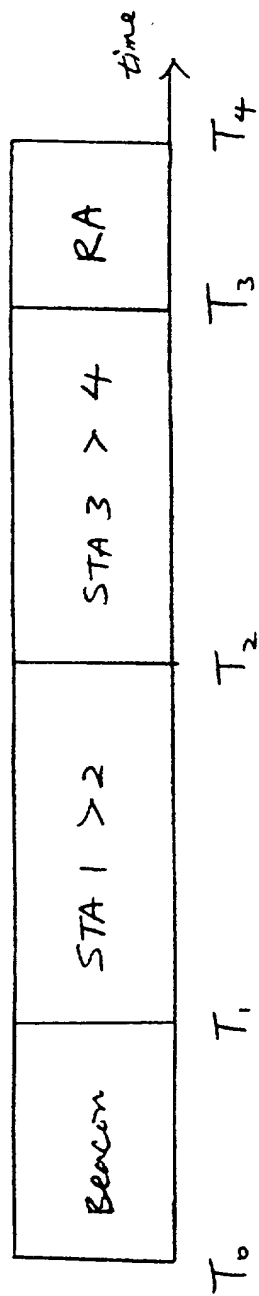
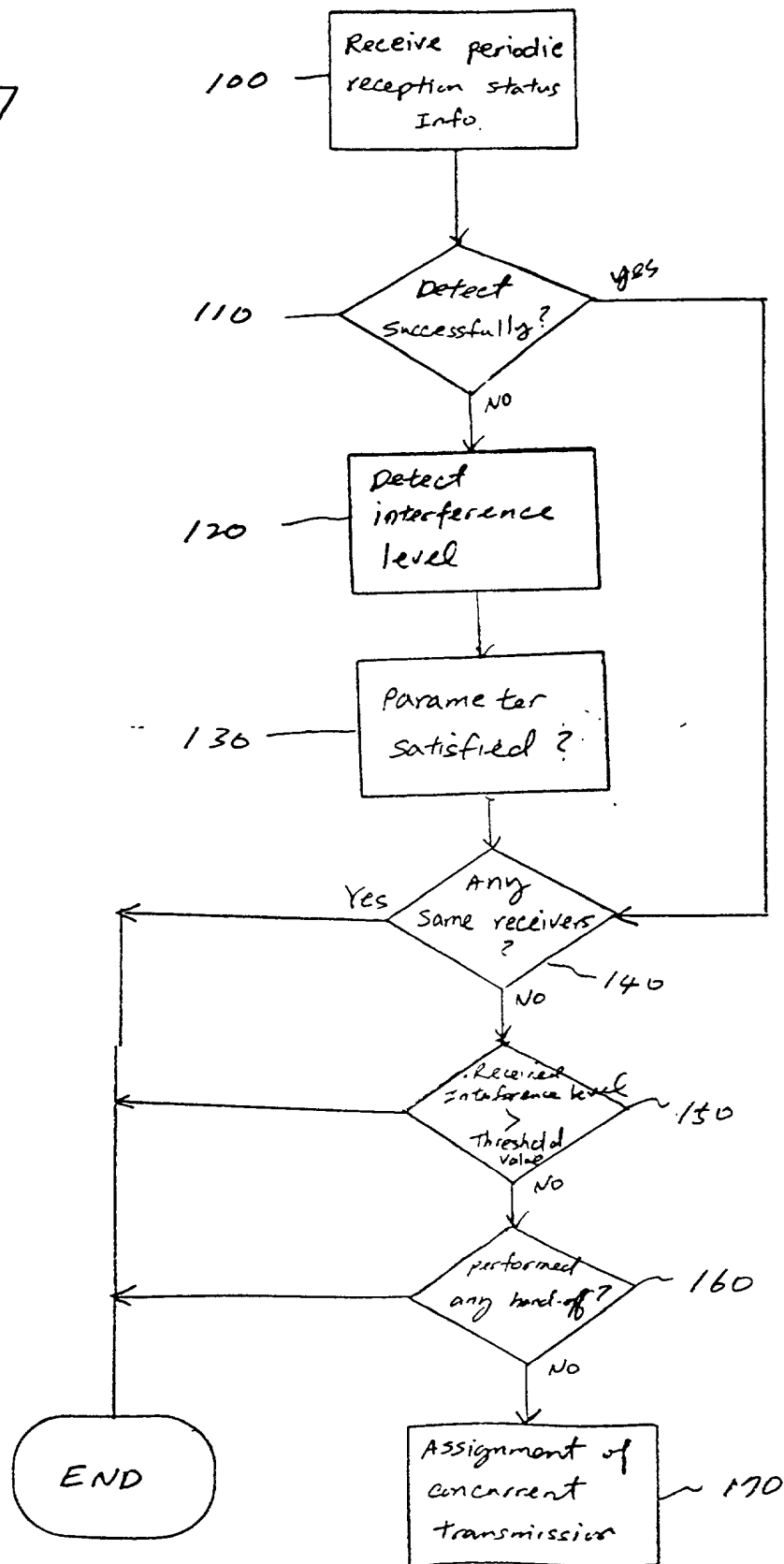


Fig. 5

Received Signal Strength (RSS)	STA 1	STA 2	STA 3	STA 4	STA N
$t_1$	$RSS_{STA1} > RSS_{th}$	$RSS_{STA2} > RSS_{th}$	$RSS_{STA3} < RSS_{th}$	$RSS_{STA4} < RSS_{th}$	- - -
$t_2$	$RSS_{STA1} < RSS_{th}$	$RSS_{STA2} < RSS_{th}$	$RSS_{STA3} > RSS_{th}$	$RSS_{STA4} > RSS_{th}$	- - -
$t_3$					

FIG. 6

FIG. 7



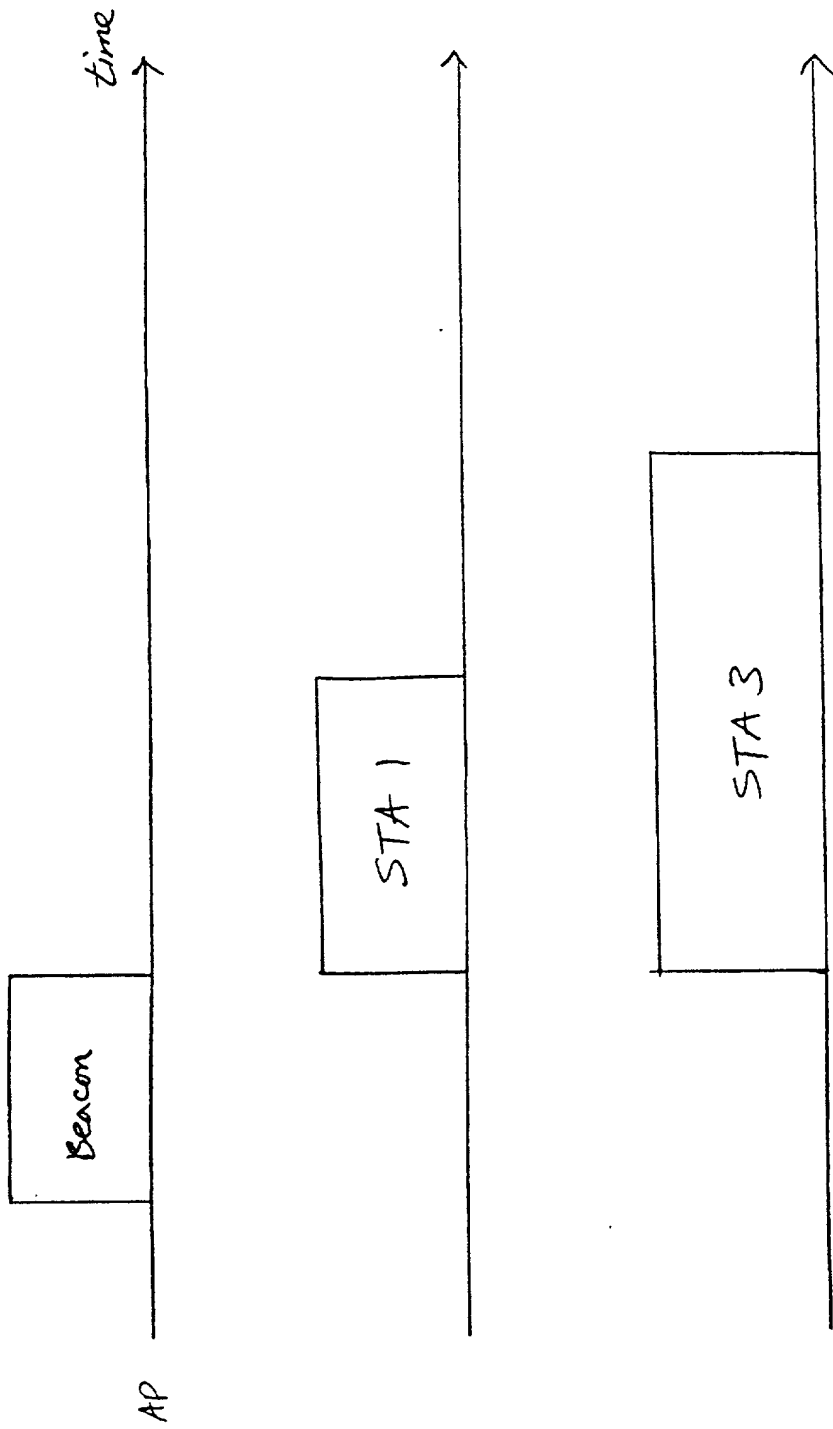


FIG. 8